REMARKS

The present Amendment amends claims 1 and 2 and leaves claims 3-10 unchanged. Therefore, the present application has pending claims 1-10.

In paragraph 2 of the Office Action the Examiner objected to the title as not being descriptive of the invention. The title of the invention was changed to "STORAGE UNIT HAVING NORMAL AND BACKUP POWER SOURCES FOR USE IN RETAINING DATA WHEN NORMAL POWER FAILS", which Applicants submit is descriptive of the present invention. Therefore, this objection is overcome and should be withdrawn.

Claim 2 stands rejected under 35 USC §112, second paragraph as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicants regards as their invention. Various amendments were made throughout claim 2 to bring it into conformity with the requirements of 35 USC §112, second paragraph. Therefore, Applicants submit that this rejection is overcome and should be withdrawn.

Specifically, amendments were made throughout claim 2 to correct the informalities noted by the Examiner in paragraphs 3 and 4 of the Office Action.

Claims 1, 7 and 8 stand rejected under 35 USC §102(b) as being anticipated by Fujita (U.S. Patent No. 5,359,569); and claims 2-6, 9 and 10 stand rejected under 35 USC §103(a) as being unpatentable over Fujita. These rejections are traversed for the following reasons. Applicants submit that the features of the present invention as now more clearly recited in claims 1-10 are not taught or suggested by Fujita whether taken individually or in combination with any of the other references of record. Therefore, Applicants

respectfully request the Examiner to reconsider and withdraw these rejections.

Amendments were made to claim 1 from which claims 2-10 depend so as to more clearly describe features of the present invention. Particularly, amendments were made to the claims so as to recite that the present invention is directed to a storage unit including a storage device to store data, a storage device control section to control the writing/reading of the data to/from the storage device, a channel control section to control an interface with a host machine, a cache memory to temporarily store the data written/read between the host machine and the storage device, a first power source to supply, to the cache memory, a voltage in a normal operation mode in which the data is written to/read from the cache memory, and a second power source to supply, to the cache memory, a voltage in a backup operation mode in which the data stored in the cache memory is retained.

Unique according to the present invention as now more clearly recited in the claims is that upon occurrence of a failure in the first power supply, the storage unit reduces the voltage of the normal operation mode supplied by the first power source to the cache memory, starts a destaging process in which data in the cache memory is stored in the storage device, and switches, after the destaging process has been completed, the operation mode of the cache memory from the normal operation mode to the backup operation mode in which the voltage of the backup mode is supplied by the second power source to the cache memory.

The above described features of the present invention now more clearly recited in the claims are not taught or suggested by any of the

references of record whether taken individually or in combination with each other. Particularly, the above described features of the present invention are not taught or suggested by Fujita.

Fujita teaches a semiconductor storage, for example, as illustrated in Fig. 1 having a main flash memory 2, a write memory 3, a data control circuit 4, a battery 6 and a power supply unit 7. Fujita teaches that when a read instruction of data is sent from a processing apparatus, the data control circuit 4 reads out data added with an Error Check Code (ECC) at a designated address of the main flash memory 2, and that when a write instruction of data is sent from the processing apparatus, the data added with an ECC is written into the cache memory 3 via the data control circuit 4 and then subsequently written into the area of the relevant address of the main flash memory 2.

Fujita further teaches that the power supply unit 7 supplies power to each section of the semiconductor memory and also charges the battery 6, and that the battery 6 supplies power to the main flash memory 2, write cache memory 3 and data control circuit 4 in place of the power supply unit 7 when the power supply of the power supply unit 7 is cutoff or a failure occurs.

However, at no point in Fujita is there any teaching of the above described features of the present invention now more clearly recited in the claims. Particularly, at no point is there any teaching or suggestion in Fujita that upon detection of an occurrence of a failure in a normal operation power supply, the voltage being supplied by the normal operation power supply is reduced to conserve power but not prevent the cache memory to continue somewhat normal operation so that data can be properly stored and retained. As discussed in the specification, for example in the paragraph bridging pages

31 and 32, this reduction allows for various subsequent operations to be performed including the sequentially power down of various portions of the storage unit and the destaging of data from the cache memory to the storage device. At no point is there any teaching or suggestion in Fujita that, upon the occurrence of a failure, the voltage being supplied to the cache memory in the normal operation mode is reduced, and various subsequent operations are performed including the sequential powering down of various portions of the storage unit and the destaging of data from the cache memory to the storage device as in the present invention.

Further, there is no teaching or suggestion in Fujita that once the destaging process has been completed, the storage unit switches, after the destaging process has been completed, the operation mode of the cache memory from the normal operation mode to the backup operation mode in which the voltage of the backup mode is supplied by the second power source to the cache memory as in the present invention.

Still further there is no teaching or suggestion in Fujita that the cache memory is switched from a normal operation mode to a backup operation mode and that different voltages are supplied so as to operate the cache memory in the different operation modes as in the present invention. In fact there is no teaching or suggestion in Fujita that the write cache memory 3 operates in two different operation modes corresponding to the cache memory of the storage unit of the present invention as recited in the claims.

In Fujita the battery is simply provided to maintain power in the volatile memory (Flash memory) to prevent it from becoming volatile and to allow the flash memory to retain data even when external power is not supplied. There

is no teaching or suggestion in Fujita that the voltage supplied by the battery is part of a method of operating the write cache memory 3 in two different operation modes as in the present invention. The use of the battery as taught by Fujita is a typical flash memory configuration that has no relationship to the problem to which the present invention as now recited in the claims is directed.

Thus, Fujita fails to teach or suggest that upon occurrence of a failure in said first power supply, said storage unit reduces said voltage of said normal operation mode supplied by said first power source to said cache memory, starts a destaging process in which data in said cache memory is stored in said storage device, and switches, after said destaging process has been completed, the operation mode of said cache memory from said normal operation mode to said backup operation mode in which said voltage of said backup mode is supplied by said second power source to said cache memory as recited in the claims.

Therefore, the above described features of the present invention as now more clearly recited in the claims are not taught or suggested by Fujita whether taken individually or in combination with any of the other references of record. Accordingly, reconsideration and withdrawal of the 35 USC §102(b) rejection of claims 1, 7 and 8 as being anticipated by Fujita and the 35 USC §103(a) rejection of claims 2-6, 9 and 10 as being obvious over Fujita is respectfully requested.

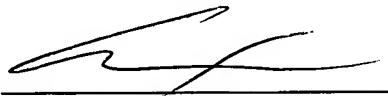
The remaining references of record have been studied. Applicants submit that they do not supply any of the deficiencies noted above with respect to the reference utilized in the rejection of claims 1-10.

In view of the foregoing amendments and remarks, applicants submit that claims 1-10 are in condition for allowance. Accordingly, early allowance of claims 1-10 is respectfully requested.

To the extent necessary, the applicants petition for an extension of time under 37 CFR 1.136. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, or credit any overpayment of fees, to the deposit account of MATTINGLY, STANGER, MALUR & BRUNDIDGE, P.C., Deposit Account No. 50-1417 (843.43760X00).

Respectfully submitted,

MATTINGLY, STANGER, MALUR & BRUNDIDGE, P.C.



Carl I. Brundidge
Registration No. 29,621

CIB/jdc
(703) 684-1120